

Abstract

A translator tool for translating simulation test data generated to test clock recovery circuitry of a device from an event-based format to a cycle-based format readable by integrated circuit testers is presented. The simulation test data includes test timing irregularities intentionally injected into a serial data signal that will be processed by the clock recovery circuitry of the device under test. The translator tool includes a normalization function that extracts the intentionally injected timing irregularities from the event-based test data and generates corresponding normalized event-based test data without the extracted timing irregularities. The translator tool includes a cyclization engine that cyclizes the normalized event-based test data to generate corresponding cycle-based test data without the timing irregularities. Preferably, the extracted timing irregularities are stored and formatted into a timing irregularities file readable by the integrated circuit tester to allow the tester to reinject the timing irregularities back into the cycle-based test data using its own timing irregularities injection tools.